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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,499	09/30/2003	Motoki Kobayashi	FUJI 137	2321

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EXAMINER	
ROSE, KIESHA L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,499	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9 and 21-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9 and 21-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the RCE filed 10 January 2006.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 21,22,24-25,27,29 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakai et al. (U.S. Patent 6,229,165).

In re claims 21 and 27, Sakai discloses an electric circuit semiconductor device (Fig. 12a) that contains a support substrate (121) including at least one groove (130), a first insulation layer (122) on top of the support substrate, an SOI layer (123) formed on top the first insulation layer, a first element layer on the SOI layer, wherein the at least one groove extends below a target element (124/126)(plurality of analog elements) in the first element layer whose dielectric loss is to be controlled (as disclosed in the applicant's specification, the dielectric loss is controlled when the substrate has a groove which thins the substrate so dielectric loss is controlled), a second insulation layer (137) formed on top the first element layer and at least one additional element layer (138) formed on top the second insulation layer (138 is an element layer because it can be connected to other semiconductor layers or circuitry) and a plurality of bonding

pads (138 (far left and far right)) surrounding the first element area and wherein no groove is formed below the plurality of bonding pads.

In re claim 22, the target element is a high frequency circuit. (Target element is a MOS transistor (Column 8, lines 29-33))

In re claims 24 and 31, the at least one groove is formed such that lower face of the first insulation layer is exposed. (Fig. 12a)

In re claim 25, the target element is an analog element. (Target element is a MOS transistor, which is detecting electric signals. Column 9, lines 11-18)

In re claim 29, one or more analog elements are elements for which control of dielectric loss is sought. (As disclosed in the applicant's specification, the dielectric loss is controlled when the substrate has a groove which thins the substrate so dielectric loss is controlled, therefore the MOS transistor would be have dielectric loss controlled)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3,6,7,9 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai et al. (U.S. Patent 6,229,165) in view of Reedy et al. (U.S. Patent 6,583,445).

In re claims 1 and 6, Sakai discloses an electric circuit semiconductor device (Fig. 12a) that contains a support substrate (121) including at least one groove (130), a first insulation layer (122) on top of the support substrate, an SOI layer (123) formed on top the first insulation layer, a first element layer on the SOI layer, wherein the at least one groove extends below a target element (124/126) in the first element layer whose dielectric loss is to be controlled, a second insulation layer (137) formed on top the first element layer and at least one additional element layer (138) formed on top the second insulation layer. (138 is an element layer because it can be connected to other semiconductor layers or circuitry) Sakai discloses all the limitations except for the support substrate to be sapphire. Whereas Reedy discloses an electronic device (Fig. 2a) that contains a sapphire substrate (24). The substrate contains sapphire because it combines electronics with optical components and permits light to emit through the substrate and it also is transparent. (Column 3, lines 38-41 and Column 5, lines 12-20) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Sakai by incorporating the substrate to be sapphire to combine electronics with optical components and permit light to emit through the substrate and it also is transparent as taught by Reedy.

In re claims 2 and 7, Sakai discloses the at least one groove is formed such that a lower face of the first insulation layer is exposed. (Fig. 12a)

In re claim 3, Sakai discloses the target element is an analog element. (Target element is a MOS transistor, which is detecting electric signals. Column 9, lines 11-18)

In re claim 9, Sakai discloses one or more analog elements are elements for which control of dielectric loss is sought, among the plurality of analog elements. (As disclosed in the applicant's specification, the dielectric loss is controlled when the substrate has a groove which thins the substrate so dielectric loss is controlled, therefore the MOS transistor would be have dielectric loss controlled)

In re claim 32, Sakai discloses the target element is a high frequency circuit. (Target element is a MOS transistor (Column 8, lines 29-33))

Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai and Reedy as applied to claims 1 and 6 above, and further in view of Eda et al. (U.S. 5,668,057).

In re claims 4 and 8, Sakai and Reedy disclose all the limitations except for the analog element to be an inductor. Whereas Eda discloses a semiconductor device (Fig. 6) that contains analog elements (3-5), which can be a transistor or an inductor. An inductor is used to act as passive chip component in the device. (Column 13, lines 25-30) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Sakai and Reedy by incorporating the analog element to be an inductor to act as a passive chip component for the device as taught by Eda.

Claims 23 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai as applied to claims 21 and 27 above, and further in view of Reedy.

In re claims, 23 and 30, Sakai discloses all the limitations except for the support substrate to be sapphire. Whereas Reedy discloses an electronic device (Fig. 2a) that contains a sapphire substrate (24). The substrate contains sapphire because it combines electronics with optical components and permits light to emit through the substrate and it also is transparent. (Column 3, lines 38-41 and Column 5, lines 12-20) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Sakai by incorporating the substrate to be sapphire to combine electronics with optical components and permit light to emit through the substrate and it also is transparent as taught by Reedy.

Claims 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai as applied to claims 21, 25 and 27 above, and further in view of Eda et al.

In re claims, 26 and 28, Sakai discloses all the limitations except for the analog element to be an inductor. Whereas Eda discloses a semiconductor device (Fig. 6) that contains analog elements (3-5), which can be a transistor or an inductor. An inductor is used to act as passive chip component in the device. (Column 13, lines 25-30) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Sakai by incorporating the analog element to be an inductor to act as a passive chip component for the device as taught by Eda.

Response to Arguments

Applicant's arguments with respect to claims 1-4,6-9 and 21-32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on T-F 8:30-6:00 off Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLR